Nolan McCleary

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Technical Skills

Languages: C, C++, Python, Verilog/SystemVerilog, MATLAB, Bash

Development Tools: Git, Make, CMake, Buildroot, Synopsys Verdi, Perforce, LTspice

Lab / Validation: JTAG, post-silicon validation, SCPI, RF Lab (SA, VNA, etc), Wirebonding

Experience

SerDes Firmware and Validation Intern
Sep 2024 – Aug 2025

Synopsys — *Toronto, Ontario*

- Led the large-scale redesign of a **JTAG-based chip validation SDK** for use on a **TSMC 3nm 224G Ethernet PHY**.
- Developed **bare-metal** calibration and channel adaptation routines in a **MISRA-C** environment.
- Optimized calibration firmware by cycle-level waveform analysis, reducing start-up critical path by **8 percent**.
- Wrote a custom **Python** script to automatically parse generated assembly files and compare used ICCM region sizes against linker-script allocations, enabling detection of over-buffered memory regions and reducing overall firmware binary size by **15 percent**.
- Refactored the **e224g** firmware codebase and migrated the build system from **Make to CMake**.
- Performed post-silicon validation of firmware calibrations and channel adaptations on a **TSMC 3nm** test chip; analyzed eye diagrams, histogram/scatter plots, and bathtub curves to debug chip-level issues and quantify firmware improvements.

Embedded Software Intern
May 2023 – Aug 2023

General Dynamics — *Ottawa, Ontario*

- Developed Linux userspace drivers in **C++** to acquire, decode, and stream critical **Xilinx Zynq UltraScale+ MPSoC** information over **TCP** through a series of custom **JSON-RPC API endpoints**; exposed real-time processor temperature telemetry, Quad SPI (QSPI) partition boot status, and boot binary checksums.
- Engineered an automated build system via **Buildroot** to allow a consolidated **UltraScale+ device core** to be built; built artifacts included an embedded Linux kernel (**PetaLinux**), FPGA image, bootloader, root filesystem, and all relevant bare-metal applications.
- Created a **GitLab CI/CD** pipeline using this build system to perform static code analysis on the firmware core across all used Xilinx toolchains concurrently, accelerating new core feature integration.

Embedded Systems Intern
May 2022 – Dec 2022

Teck Resources Limited — *Sparwood, BC*

- Designed, built, and tested a remote voltage spike suppression and detection system with high-speed transient capture, Ethernet networking, and dynamic system network parameter reconfiguration over Ethernet.
- Deployed the voltage monitor across **four sites**; the system helped suppress and identify the source of previously unidentified transients at operationally critical locations inside heavy equipment, preventing up to **$100,000** in lost throughput.

Projects

Real-Time Operating System (RTOS)
June 2026 - Oct 2026

Source code and documentation

- Designed and implemented a bare-metal **dual-core RTOS** for the ARM Cortex-A9 (Cyclone V SoC), written from scratch in **C and ARM assembly**.
- Developed a hybrid **Earliest-Deadline-First (EDF) / priority round-robin scheduler** with per-core deadline and release-time heaps, periodic task management, and utilization-based SMP task placement.
- Implemented ARM exception vectors, **IRQ/FIQ interrupt handlers**, and preemptive context switching in assembly, including register preservation, exception-frame construction, and atomic CPSR/PC restoration.
- Engineered a standalone **dual-core boot and BSP initialization sequence**, including SDRAM PHY calibration, MMU page tables, L1/L2 cache configuration, SCU coherency, GIC/timer setup, and inter-core synchronization.

FPGA-Based Pound-Drever-Hall Laser Frequency Lock for Photonic IC Oct 2025 – April 2026

Source code and documentation

- Associated with the **UBC System On Chip (SoC) lab**. Implemented a real-time **Pound-Drever-Hall laser frequency stabilization system** on a **Xilinx Zynq XC7Z010 SoC** for use on a **custom photonic integrated circuit**.
- Developed **SystemVerilog** modules for **NCO-based IQ demodulation**, **high-speed PID control**, programmable **FIR filtering**, dual-clock BRAM buffering, and **AXI3 DMA** live capture for high-speed, nondestructive capture of real-time control and signal processing metrics.
- Implemented **Embedded Linux** networking and control code for high-level management of the RTL from the SoC's Hard Processor over a **custom Application Binary Interface**, and a custom TCP-based remote procedure call API and GUI for client-side control of the system from a laptop.
- Validated the full stack with **cocotb**, Verilator/Icarus simulation, and board-level regression tests covering callback correctness, fixed-point coefficient programming, filter-response behavior, loopback validation, and DMA data-path integrity.
- Constructed prototype test infrastructure using DFB laser diodes, fiber optics, electro-optic modulators, beam splitters, and lightwave converters for early-stage testing of the control system before the photonic IC was available.

RC4 Decryption Engine June 2024

Source code and documentation

- Used **SystemVerilog** to develop a custom decryption engine implementing the **RC4 stream cipher** on an **Altera Cyclone V FPGA**.
- Parallelized the decryption process across **90 individual decryption cores**, greatly accelerating performance and successfully breaking encrypted messages with key lengths of up to **28 bits**.
- Implemented a pipelined architecture to support higher reference clock frequencies during many-core builds.

Laser Projector Feb 2024 – Apr 2024

Source code and documentation

- Designed, programmed, and tested an **ARM MCU-based vector-scan laser projector**.
- Utilized hardware timers, interrupts, and digital filtering to facilitate hard real-time PID control of the laser beam via the simultaneous operation of two DC motors.
- Employed **DMA** along with hardware buffering to ensure reliable high-speed acquisition of laser coordinate data over a USART connection, enabling real-time streaming of arbitrarily large laser image files without storing image data in controller flash.

Education

University of British Columbia Vancouver, BC

Bachelor of Applied Science in Electrical Engineering *2026*